EA TFT024-23ATNN

INCL CONTROLLER ST7789

Dimension 42.7 x 60.3 x 3.1mm

FEATURES

- 240x320 DOTS (COLOR AND MONOCHROME)
- HIGH CONTRAST TFT DISPLAY
- LOW POWER WITH 35mw ONLY (W./O. BACKLIGHT)
- TRANSFLECTIVE MODE
- SUNLIGHT READABLE
- PERFECT FOR MOBILE APPLICATIONS
- SPI INTERFACE: MOSI, CLK, CS, D/C
- WIDE TEMPERATURE RANGE (T_{OP} -20°C - +70°C)

ORDERING CODE

• GRAPHIC 240x320, COLORED TFT	**EA TFT024-23ATNN**

ACCESSORIES

• ZIFF CONNECTOR 0.3mm, BOTTOM CONTACT	**EA WF030-39S**
• 50 mm EXTENSION CABLE 0.3mm	**EA KF030WF-39L50**
• BREAK-OUT BOARD 2.54 mm CONTACTS	**EA 9980-TFT**

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Issue 06.2024

1. REVISION HISTORY

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGEDBY
A	2024.01.31	First Release.	Huang Chun Liang
	2024.06.10	Adding some accessories	RT

2. CONTENT

Content

3. GENERAL DESCRIPTION

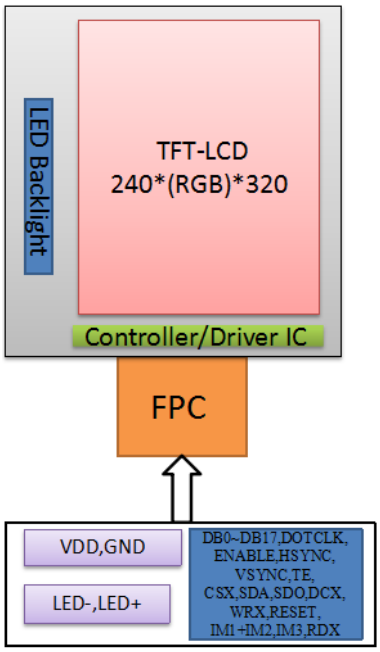
EA TFT024-23ATNN is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). The module display area contains 240 (RGB) × 320 pixels. This product accords with RoHS environmental criterion.

Display is transflective type which means that it an be used without backlight. Compared to other TFT display technologies a bright ambient backlight (especially outside, sunlight) makes the display brighter and helps to improve contrast for reading.

Parameter		Specifications	Unit
Screen size		2.4(Diagonal)	inch
Resolution		240 (RGB) × 320	Pixel
Active area		36.72(H) x 48.96(V)	mm
Outline dimension		42.72(H) x 84.26(V) x 3.05(D)	mm
Display Mode		Normally White/Transflective	-
Driving method		TFT active matrix	-
Pixel pitch		0.153(H) × 0.153(V)	mm
Controller		ST7789T3-G	
Input Signals		RGB, 8080-8bit, SPI, 8080-16bit	-
Display Color		262K	-
View Angle direction		10:00	-
Temperature Range	Operation	-20~+70	℃
	Storage	-30~+80	℃
Brightness		270	cd/m²
Input voltage		3.0±0.3	V
RoHS Compliance		RoHS	-

4. BLOCK DIAGRAM

The following diagram shows the function block of the 2.4 inch color TFT-LCD module:



5. INTERFACE PINOUT

Pin	Symbol	Function	Remark
1	LED-	Cathode of the backlight.	
2	LED+	Anode of the backlight.	
3	VDD	Power Supply.	
4	GND	Power Ground.	
5~22	DB0~DB17	-DB[17:0] are used as MCU parallel interface data bus. 8080 8-bit I/F: when IM3:0, DB[7:0] are used; 8080 16-bit I/F: when IM3:1, DB[17:10] and DB[8:1] are used. -DB[17:0] are used as RGB interface data bus. 6-bit RGB I/F: DB[5:0] are used. 16-bit RGB I/F: DB[17:13], DB[11:1] are used. 18-bit RGB I/F: DB[17:0] are used. -If not used, please fix this pin at VDD or GND.	Note 1
23	DOTCLK	Dot clock signal for RGB interface operation. If not used, please fix this pin at VDD or GND.	
24	ENABLE	Data enable signal for RGB interface operation. If not used, please fix this pin at VDD or GND.	
25	HSYNC	Horizontal (Line) synchronizing input signal for RGB interface operation. If not used, please fix to VDD or GND.	
26	VSYNC	Vertical (Frame) synchronizing input signal for RGB interface operation. If not used, please fix to VDD or GND.	
27	TE	Tearing effect signal is used to synchronize MCU to frame memory writing. If not used, please let this pin open.	
28	CSX	Chip selection pin Low enable. High disable.	
29	SDA	When IM3: Low, 4-line serial interface input/output pin. When IM3: High, 4-line serial interface input pin. The data is latched on the rising edge of the clock signal. If not used, please fix this pin at VDD or GND	
30	SDO	4-line serial interface output pin. The data is output on the falling edge of the clock signal. If not used, let this pin open.	
31	DCX	-Display data/command selection pin in 80 parallel interface. DCX='1': display data or parameter. DCX='0': command data. -This pin is used to be 4-line serial interface clock. -If not used, please fix this pin at VDD or GND.	
32	WRX	Write enable in 80 parallel interface. Display data/command selection pin in 4-line serial interface. If not used, please fix this pin at VDD or GND.	
33	RESET	This signal will reset the device and it must be applied to properly initialize the chip. Signal is active low.	
34	IM1+IM2	The MCU interface mode select.	Note 1
35	IM3	The MCU interface mode select.	Note 1
36	RDX	Read enable in 8080 MCU parallel interface. If not used, please fix this pin at VDD or GND.	
37	NC	Not connected	
38	NC	Not connected	
39	NC	Not connected	

Note 1.MCU interface mode select:

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Connect Pin</th></tr>
<tr><td>IM3,IM2,IM1
IM0=0</td><td>I</td><td>The MCU interface mode select
<table>
<tr><th>IM3</th><th>IM2+IM1</th><th>MCU interface mode</th><th>Data Pin</th></tr>
<tr><td>0</td><td>0</td><td>80-8bit parallel I/F</td><td>DB[7:0]</td></tr>
<tr><td>0</td><td>1</td><td>4-line 8bit serial I/F</td><td>SDA:in/out</td></tr>
<tr><td>1</td><td>0</td><td>80-16bit parallel I/F II</td><td>DB[17:10],
DB[8:1]</td></tr>
<tr><td>1</td><td>1</td><td>4-line 8bit serial I/F II</td><td>SDA:in
SDO:out</td></tr>
</table></td><td>GND/VDD</td></tr>
</table>

6. ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	STANDARD	UNITS
Supply Voltage Range	VDD	-0.3 to +4.6	V
Logic input Voltage Range	VIN	-0.3 to VDD+0.5	V
Logic output Voltage Range	VO	-0.3 to VDD+0.5	V
Operating temperature Range	TOP	-20 to +70	°C
Storage temperature Range	TST	-30 to +80	

Note 1: The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

6.2 TFT-LCD MODULE CHARACTERISTICS

Item	Symbol	Conditions	Min	Typ	Max	Unit
Power supply voltage	VDD	Ta = 25 °C	2.7	3.0	3.3	V
Output Voltage	VOH	H level	0.8*VDD	-	VDD	
	VOL	L level	GND	-	0.2*VDD	
Input Voltage	VIH	H level	0.7*VDD	-	VDD	
	VIL	L level	GND	-	0.3*VDD	
Supply Current For VDD	I_{VDD}	VDD=3.0V Ta = 25 °C	-	6.4	9.6	µA

6.3 BACKLIGHT SPECIFICATION

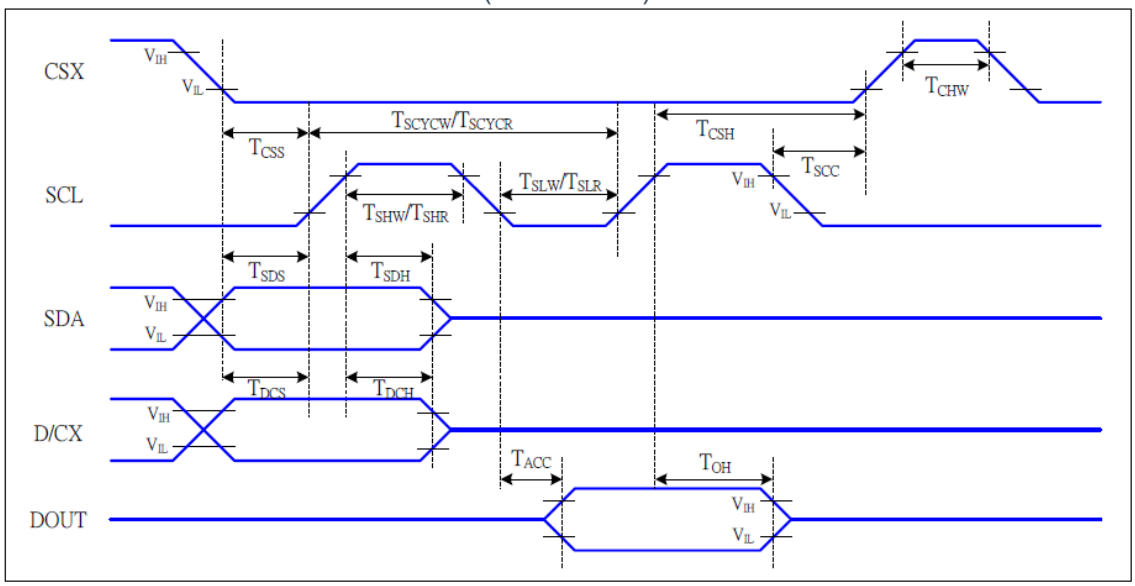
Item	Sym	Min	Typ	Max	Unit	Note
Voltage for LED backlight	V_L	-	3.0	-	V	Note 1
Current for LED backlight	I_L	-	60	-	mA	Note 2
Luminance	Lv	4500	-	9000	cd/m²	
Uniformity	Avg	80	-	-	%	
Number of LED	-	-	4	-	-	

Note 1: The LED Supply Voltage is defined by the number of LED at Ta=25℃ and IL=60mA.
Note 2: Constant current.

7. INTERFACE TIMING

7.1 AC CHARACTERISTICS

7.1.1 Serial Interface Characteristics (4-line serial)

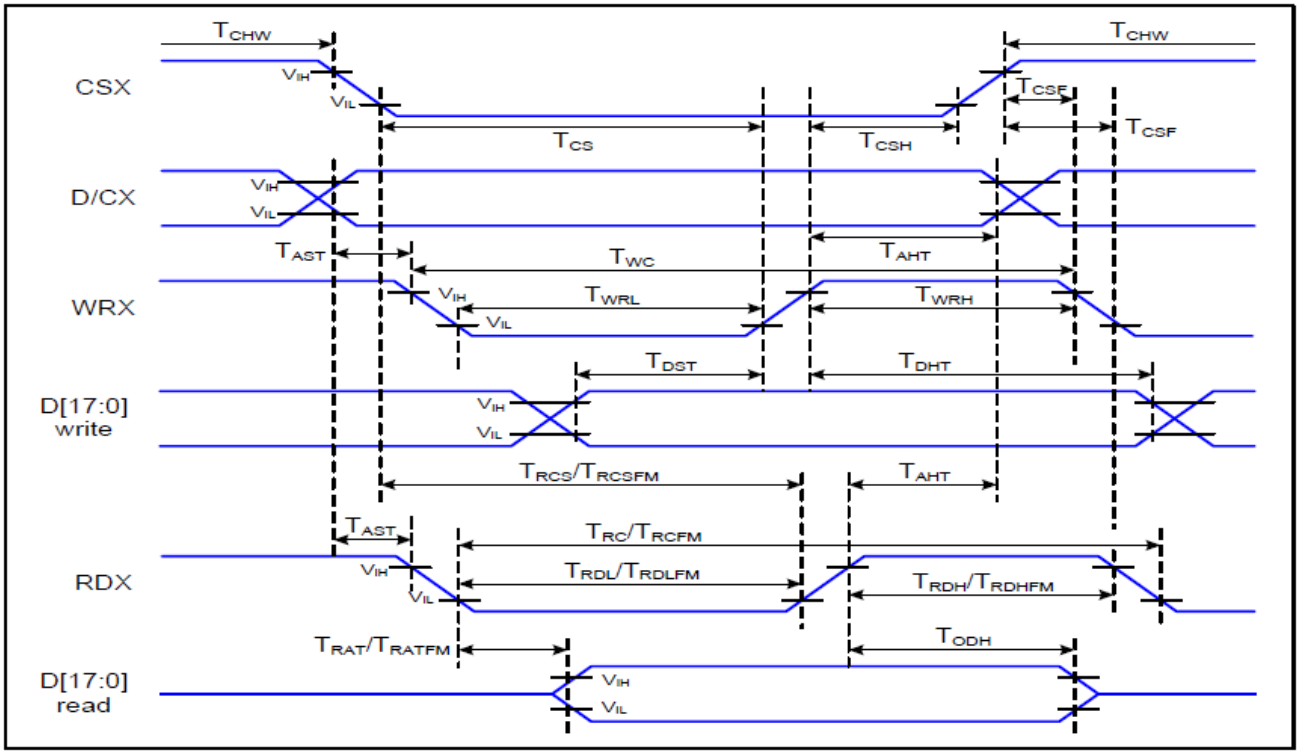


VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	7		ns	
	T_{SLW}	SCL "L" pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	7		ns	
	T_{SDH}	Data hold time	7		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

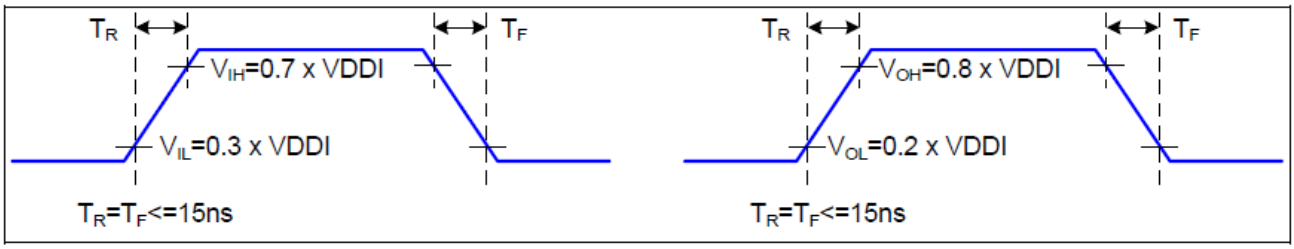
Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15ns or less. Logic high and low levels are specified as 30% and 70% of VDD for Input signals.

7.1.2 8080 Series MCU Parallel Interface Characteristics: 16/8-bit Bus

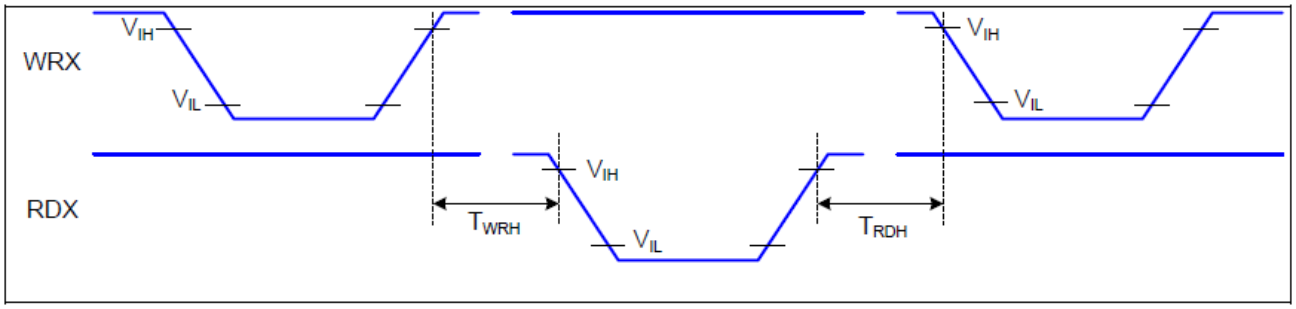


VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse "H" duration	15		ns	
	T_{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF



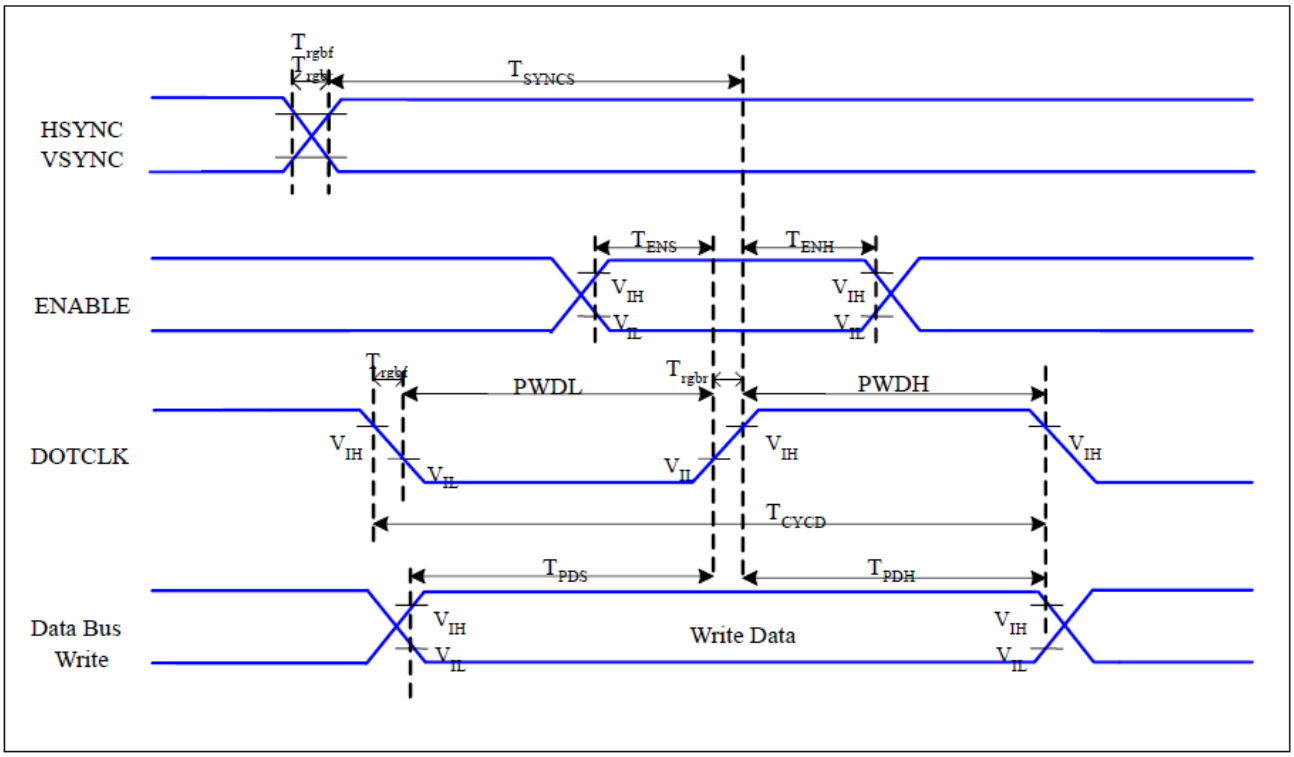
Rising and Falling Timing for I/O Signal



Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.1.3 RGB Interface Characteristics



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

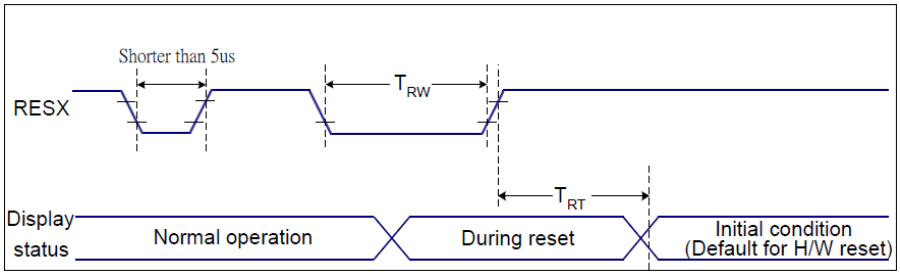
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	20	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{PDH}	PD Data Hold Time	50	-	ns	

18/16 Bits RGB Interface Timing Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	35	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	35	-	ns	
	T_{ENH}	Enable Hold Time	35	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	35	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	35	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	80	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	10	ns	
DB	T_{PDS}	PD Data Setup Time	35	-	ns	
	T_{PDH}	PD Data Hold Time	35	-	ns	

6 Bits RGB Interface Timing Characteristics

7.2 RESET TIMING



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

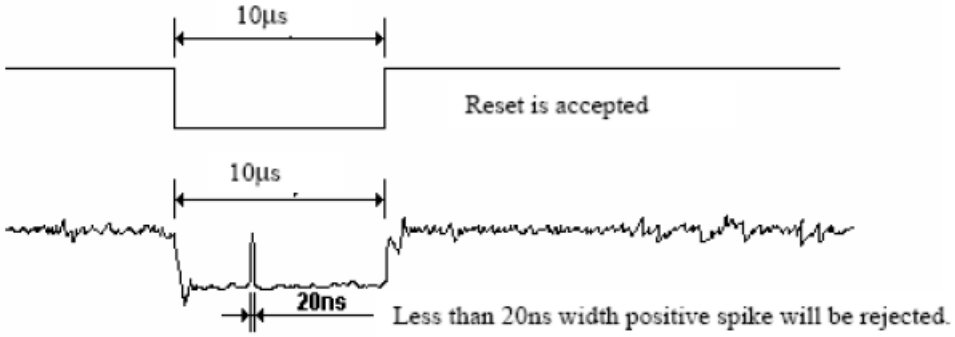
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out-mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware.
Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

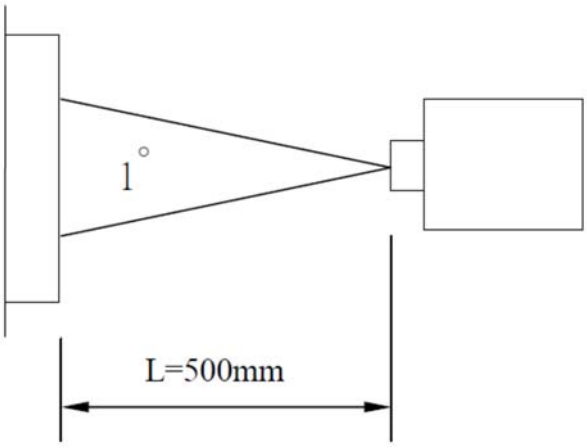
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. OPTICAL CHARACTERISTICS

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 30 minutes in a dark environment at 25 ℃. The values specified are at an approximate distance 500mm from the LCD surface at a viewing angle of Φ and θ equal to 0°.

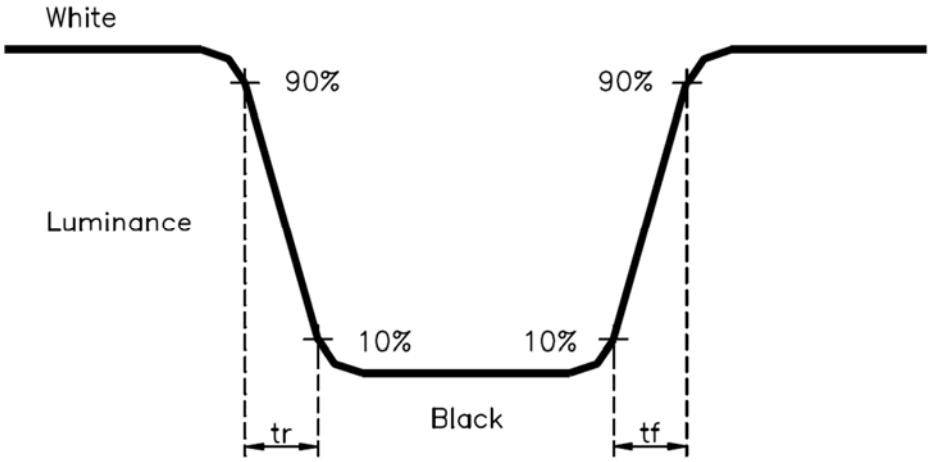
Item		Condition	Values			Unit	Note
			Min	Typ	Max		
Contrast Ratio		Center	-	15	-	-	Note(3)
Response time		$T_{ON}+T_{OFF}$	-	6	8	ms	Note (4)
Viewing Angle (CR＞2)	Hor	θ_L	-	60	-	Degree	Note(5)
		θ_R	-	60	-		
	Ver	θ_U	-	60	-		
		θ_D	-	60	-		
Chromaticity		Wx	Typ-0.05	0.314	Typ+0.05	-	Note(2,6,7)
		Wy		0.326		-	
		Rx		0.475		-	
		Ry		0.297		-	
		Gx		0.338		-	
		Gy		0.483		-	
		Bx		0.170		-	
		By		0.124		-	
LCD Surface Luminance		L	-	270	-	cd/㎡	Note(7)

Note 1.Test Conditions: VDD=3.0V, IL=60mA (Backlight current).
Ambient condition：25℃±2℃, 60±10%RH, under 10 Lux in the darkroom.
Note 2.Measure device：BM-5A (TOPCON), viewing cone=1°.

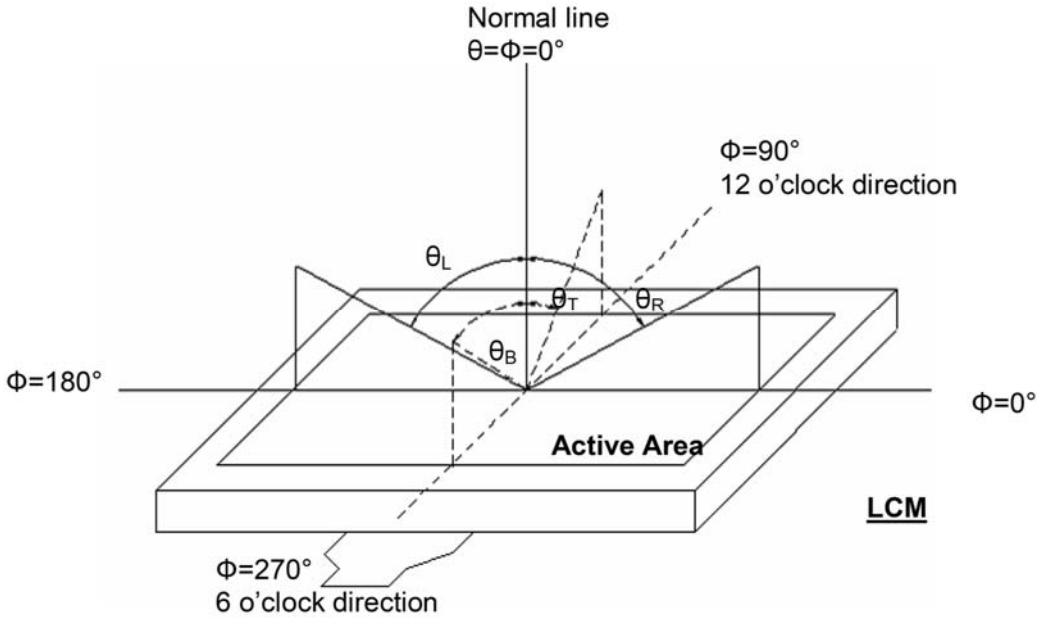


Note 3.Definition of Contrast Ratio : CR = White Luminance (ON) / Black Luminance (OFF)

Note 4.Definition of response time : The response time is defined as the time interval between the 10% and 90% amplitudes.



Note 5.Definition of view angle(θ, Φ) :



Note 6. Definition of color chromaticity (CIE1931), Color coordinates measured at center point of LCD.

Note 7. The LED driving condition is IL=60mA.

9. RELIABILITY TEST

No.	Test Items	Test Condition	Remark
1	High Temperature Storage Test	Ta=+80℃ Dry 240h	
2	Low Temperature Storage Test	Ta=-30℃ Dry 240h	
3	High Temperature Operation Test	Ta=+70℃ Dry 240h	
4	Low Temperature Operation Test	Ta=-20℃ Dry 240h	
5	High Temperature and High Humidity	Ta=+60℃ 93%RH 240h	Non-operating
6	Thermal Shock Test (non-operating)	-30℃(0.5h) ~ 80℃(0.5h)/100 cycles. Start with cold temperature, End with high temperature.	
7	Vibration Test	Acceleration : 5G Vibration Frequency : 10~500Hz X,Y,Z for Each 30 minutes	
9	Electro Static Discharge Test	Panel surface / top case. Contact / Air：±8KV / ±12KV， 150pF，330Ω	Non-operating

** Ta= Ambient Temperature*

Note:

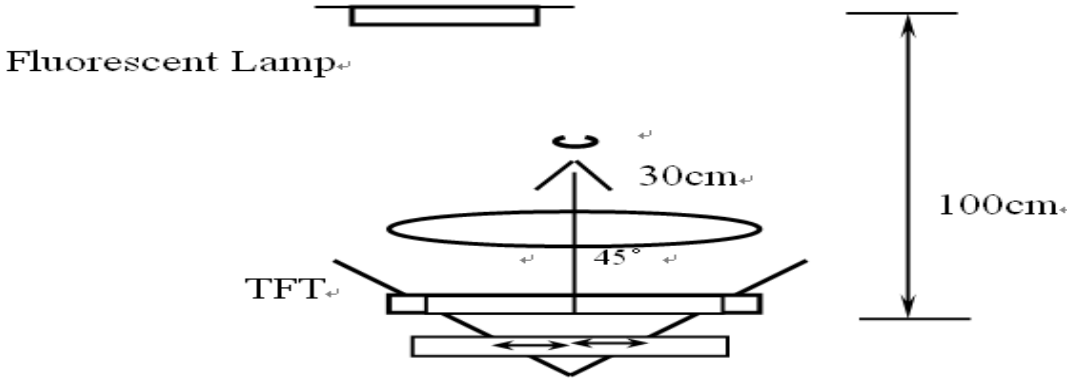
1. The test samples have recovery time for 2 hours at room temperature before the function check. In the standard conditions, there is no display function NG issue occurred.

2. All the cosmetic specifications are judged before the reliability stress.

10. QUALITY

10.1 INSPECTION METHOD

An appearance inspection should be conducted at 30 cm or more distance/height from the inspector's eye sight to the LCD module surface under fluorescent light. The distance between LCD and fluorescent lamps should be 100 cm or more. Viewing angle for inspection is 45° from vertical against LCD.



10.2. QUALITY LEVEL

The AQL for major and minor defects is defined as follows:

Partition	Definition	AQL
Major defect	Functional defective in product.	0.65
Minor defect	Meet all functions of product but have some cosmetic defective	1.0

10.3 DEFINITION

10.3.1 The environmental condition of inspection

1) Ambient temperature ：22℃±5℃， 65±20%RH
2) Function inspection：less than 200-300Lux
3) Visual inspection：750±150Lux
4) Total inspection time:in 15s

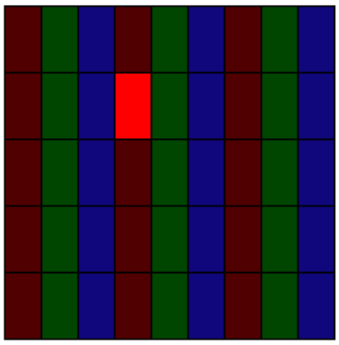
10.3.2 Definition of dot defect

The size of a defective dot full of a whole dot， and all bright dot or dark dot defect must be visible through ND 5% filter.

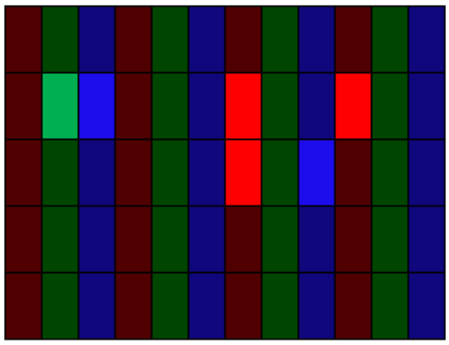
Bright dot

Dots（Sub-pixel＞1/2dot）appear bright and unchanged in size when TFT is displaying.

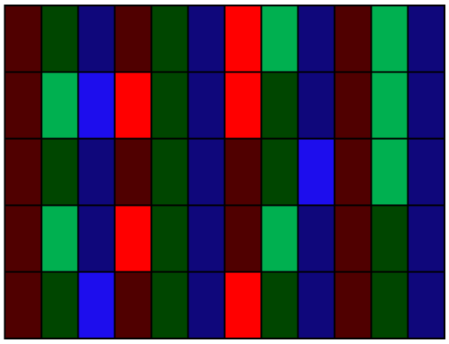
single dot



two adjacent dots



three adjacent dots



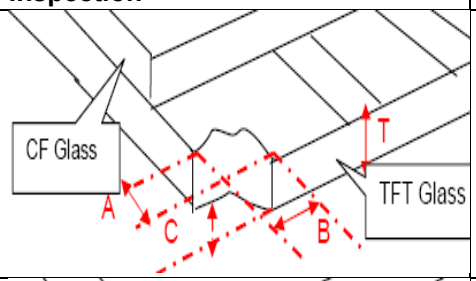
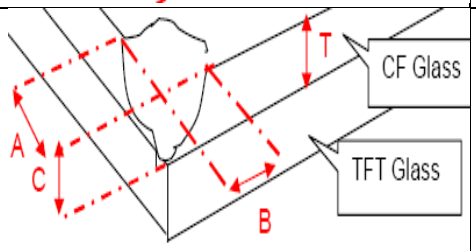
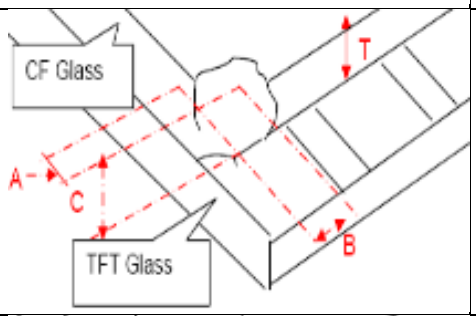
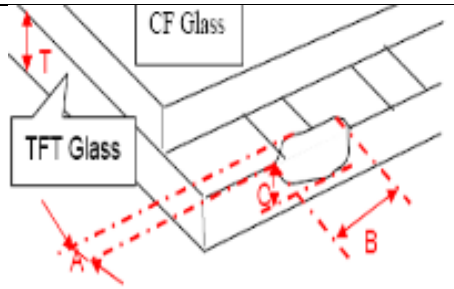
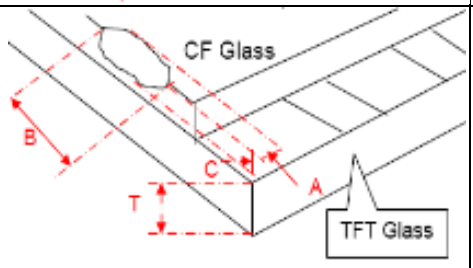
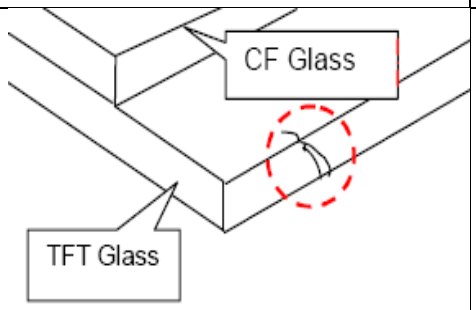
Dark dot

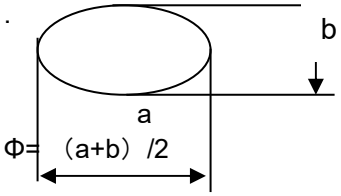
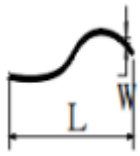
The same definition of bright dot, but always display dark

The usage of ND 5%

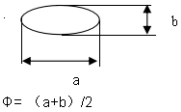
Use the ND 5% to cover bright dot within 2s,it should be judged OK if it’s invisible.

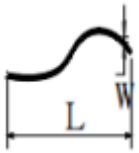
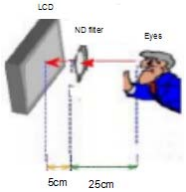
10.4. VISUAL INSPECTION STANDARD

Defect	Inspection	Criteria
1 Corner Broken **(Minor)**		1.A≤2.0 mm , B≤2.0 mm ,C≤T Ignore (No effect on function) 2. A＞2.0 mm ,or B＞2.0 mm, Not allowed
2 Corner Broken **(Minor)**		1. A≤1.5 mm , B≤1.5 mm , C≤T Ignore (No effect on function) 2. A＞1.5 mm, or B＞1.5 mm Not allowed 3. To be applied to both CF and TFT glass
3 Corner Broken **(Minor)**		1. A≤1.5 mm , B≤1.5 mm , C≤T Ignore (No effect on function) 2. A＞1.5 mm, or B＞1.5 mm Not allowed 3. To be applied to both CF and TFT glass
4 Pad Broken **(Minor)**		1. A≤0.8 mm, C≤T Ignore B Length Ignore (No effect on function) 2. A＞0.8 mm, Not allowed
5 Side Broken **(Minor)**		1. A≤0.8 mm, C≤T Ignore B Length Ignore (No effect on function) 2. A＞0.8 mm, Not allowed
6 Glass crack **(Major)**		Not allowed

<table>
<tr>
<td>7
Spot defect:
(Minor)</td>
<td>Foreign/Black/White/Bright
Spot/POL dent or bubble
 
</td>
<td>
<table>
<tr><th>Dimensions</th><th>Acceptable Numbers</th></tr>
<tr><td>Φ≤0.1mm</td><td>Ignore</td></tr>
<tr><td>0.1mm＜Φ≤0.20mm</td><td>2</td></tr>
<tr><td>0.2mm＜Φ≤0.30mm</td><td>1</td></tr>
<tr><td>Φ＞ 0.30mm</td><td>0</td></tr>
</table>
Note:
*1:defect that beyond AA area Ignored</td>
</tr>
<tr>
<td>8
Line defect
(Minor)</td>
<td>Scratch ;
Fiber
 
</td>
<td>Scratch：
<table>
<tr><th>Dimensions</th><th>Acceptable Numbers</th></tr>
<tr><td>W≤0.03mm</td><td>Ignore</td></tr>
<tr><td>L≤5 mm
0.03mm＜W≤0.05mm</td><td>2</td></tr>
<tr><td>L≤5 mm
0.05mm＜W≤0.1mm</td><td>1</td></tr>
<tr><td colspan="2">Beyond Above, Not Allowed</td></tr>
</table>
Fiber:
<table>
<tr><th>Size</th><th>Acceptable Numbers</th></tr>
<tr><td>W≤0.03mm</td><td>Ignore</td></tr>
<tr><td>L≤3 mm
0.03＜W≤0.05mm</td><td>2</td></tr>
<tr><td colspan="2">Beyond Above, Not Allowed</td></tr>
</table>
Note:
*1：defect that beyond AA area Ignored</td>
</tr>
<tr>
<td>9
(Major)</td>
<td>IC/FPC</td>
<td>1. the line broken off reject
2. oxidation/broken/fold-injury in acute angle / distortion on golden fingers reject
3. FPC protection cover fix no good or deflection over the drawing request reject
4.gold-fingers scratch/ particle/ just color difference(non-oxidation) that didn’t affect display Ignored
5.Dot or line mark that created by connector Ignored
6. Dark or white dot apply to spot defect Criteria</td>
</tr>
<tr>
<td>10
(Minor)</td>
<td>Backlight</td>
<td>1.The size don’t match with the drawing . reject
2. Surface Dirty or mark that can not wipe out Ignored
3. Scald reject
4.Uneven or Scratch on surface that doesn’t affect display Ignored</td>
</tr>
<tr>
<td>11
(Major)</td>
<td>Weld</td>
<td>1.tack weld reject
2.welding short out reject
3.very little or too much tin reject
4.FPC cock reject</td>
</tr>
<tr>
<td>12
(Minor)</td>
<td>protection film</td>
<td>Neglect any defect on protect film, such as: scratches/bubbles/particles</td>
</tr>
</table>

10.5. ELECTRICALY INSPECTION STANDARD

<table>
<tr><th>Defect</th><th>Inspection</th><th>Criteria</th></tr>
<tr><td>1
Spot defect
(Minor)</td><td>Foreign particle/Black/ White spot/Bubble .etc.
 

Φ= （a+b）/2</td><td>
<table>
<tr><td>Dimensions</td><td>Acceptable Numbers</td></tr>
<tr><td>Φ≤0.1mm</td><td>Ignore</td></tr>
<tr><td>0.1mm＜Φ≤0.20mm</td><td>2</td></tr>
<tr><td>0.2mm＜Φ≤0.30mm</td><td>1</td></tr>
<tr><td>Φ＞ 0.30mm</td><td>0</td></tr>
</table>
Note:
*1: defect that beyond AA area Ignored</td></tr>
<tr><td>2
Line defect
(Minor)</td><td>Scratched ;
Fiber
 
</td><td>Scratch:
<table>
<tr><td>Dimensions</td><td>Acceptable Numbers</td></tr>
<tr><td>W≤0.03mm</td><td>Ignore</td></tr>
<tr><td>L≤5 mm
0.03mm＜W≤0.05mm</td><td>2, *1</td></tr>
<tr><td>L≥5 mm or W≥0.05 mm</td><td>0</td></tr>
</table>
Fiber:
<table>
<tr><td>Size</td><td>Acceptable Numbers</td></tr>
<tr><td>W≤0.03mm</td><td>Ignore , *1</td></tr>
<tr><td>L≤3 mm
0.03＜W≤0.05mm</td><td>2</td></tr>
<tr><td colspan="2">Beyond Above, Not Allowed</td></tr>
</table>
Note:*1:defect that beyond AA area Ignored</td></tr>
<tr><td>3
(Minor)</td><td>Bright/dark dot
By sub-pixel</td><td>
<table>
<tr><td>Dimensions</td><td>Acceptable Numbers</td></tr>
<tr><td>Single bright dot</td><td>N ≤1</td></tr>
<tr><td>Two adjacent bright dots</td><td>reject</td></tr>
<tr><td>Three adjacent bright dots</td><td>reject</td></tr>
<tr><td>Single dark dot</td><td>≤2</td></tr>
<tr><td>Two adjacent dark dots</td><td>≤0</td></tr>
<tr><td>Three adjacent dark dots</td><td>reject</td></tr>
</table>
1:Total dot≤2</td></tr>
<tr><td>4
(Minor)</td><td>Tiny Bright dot</td><td>Invisible by ND5% Filter, Ignore;
If visible, Φ≤0.1mm, Ignore ;
0.1mm＜＜Φ≤0.30mm,N≤2</td></tr>
<tr><td>5
(Major)</td><td>Display</td><td>1.Missing segment, missing word reject
2.no display. reject
3. Viewing angle not right. reject
4. Display abnormal reject</td></tr>
<tr><td>6
(Major)</td><td>Mura/ hot spot/ Light leak (apply to all patterns)</td><td>judge by ND5% filter or limit sample
 
</td></tr>
</table>

7 (Major)	flicker	judge by ND 5% filter in grey pattern or limit sample
8 (Major)	Electricity parameter（ VoP/Current）	Over the production SPEC reject
9 (Major)	Backlight	1、 LED died off reject 2、 Display on uniformity Invisible by ND5% filter 3、 Brightness does not match the SPEC reject 4、light leak Invisible by ND5% filter
10 (Major)	Cross talk	Limit sample

11 QUALITY ASSURANCE

11.1 when customer receive our product if there is any broken on package or other quality problem, please contact us in time.

11.2 DISPLAY VISIONS will only replace or repair any of its LCD which is found defective electrically or visually when inspected in accordance with the LCM specification, for a period of one year from the date of shipment. Confirmation of such date shall be based on freight documents.
No warranty can be granted if any of the precautions stated in handing LCD and LCD Modules above have been disregarded.

11.3 In returning the LCD and LCD Modules, they must be properly packaged and there should be detailed description of the failures or defects. Broken glass, scratches on polarizers, mechanical damages as well as defects that are caused by accelerated environmental tests are excluded from warranty.

11.4 Don’t apply excessive force on the display surface;

11.5 LC is harmful material, when it leaks out, please do not touch it directly;

11.6 Store in dark places and do not expose to sunlight or fluorescent light. Keep the temperature between 0°C and 40°C and the humidity lower than 60%RH. Please consult DISPLAY VISIONS for other storage requirements.

11.7 Please do not scratch or make POL dirty. No sticker on display surface are allowed.

11.8 To avoid ESD, please keep product Storing in anti-static electricity container.

11.9 Quality assurance period is 1 year

ACCESSORY EA WF030-39S

The 39-pin FPC cable is an all in one connection. It provides all signals for

- TFT interface
- LED backlight
- PCAP touchpanel

EA WF030-39S is a 39-pin ZIFF connector for bottom side contact.

Datasheet: https://www.lcd-module.de/eng/pdf/zubehoer/WF030-39S.pdf

ACCESSORY EA KF030WF-39L50

There's a FPC cable available to extend the display connection. It's 50mm long and provides 39 pins.

12. DIMENSION